REMARKS

Applicant respectfully requests reconsideration of the subject application in light of these remarks. Claims 1, 11, 19, 20, 25, 32, 38, and 52 were previously amended and claims 27, 36-37, and 41-51 were previously canceled. As a result, claims 1-26, 28-35, 38-40, 52, and 53 are now pending and provided above for the Examiner's ease of reference.

Withdrawn Objection

Applicant hereby acknowledges and thanks Examiner Verbrugge for withdrawing the objection to claim 20 under 37 C.F.R. §1.75.

Outstanding Rejections

Claims 1, 2, 4-8, 10, 11, 12, 14-18, 26, 28, 29, and 31 stand rejected under 35 U.S.C. §102(b) as being anticipated by "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al. (hereinafter "Ohsawa").

Claims 1-5, 7, 8, 10-16, 18-20, 23-26, 29, 31-33, 35, 38-39, 52, and 53 stand rejected under 35 U.S.C. §102(e) over Boyer et al. (hereinafter "Boyer").

Claims 6, 9, 17, 21, 22, 28, 30, 34, and 40 stand rejected under 35 U.S.C. §103(a) over Boyer in view of Ohsawa.

Claims 3, 9, 13, 19, 21-25, 30, 32-35, 38-40, 52, and 53 stand rejected under 35 U.S.C. §103(a) over Ohsawa in view of Boyer.

Rejection Based on Boyer

Applicant would like to thank Examiner Verbrugge for clarifying the reasons for rejections over Boyer. It is, however, respectfully requested that the Examiner reconsider the rejections at least in light of the following remarks.

More particularly, the undersigned appreciates the Examiner's honesty in stating that "Boyer is not explicit in showing that his use registers are implemented adjacent to the memory cells" (see, outstanding Office Action at page 9, last paragraph). On page 10, first full paragraph, the outstanding Office Action goes on to state that:

> [W]hether Boyer actually shows the use registers or history bits physically adjacent to the memory rows is secondary in importance. Of primary importance is the fact that Boyer teaches that each row has an associated history bit and use register and this one-to-one logical relationship or association is what is crucial to his invention. [Emphasis Added.]

In response, it is respectfully submitted that whether an element is "crucial" to Boyer is of no interest in considering the patentability of the claimed combination of features as set forth in the pending claims. Moreover, if having history/valid bits adjacent to a memory device is of no interest to Boyer, it clearly points out that Boyer does not anticipate the claimed combination of features such as set forth in the pending claims of the present application.

For example, the Examiner is kindly invited to review Fig. 5 and the corresponding detailed description section of the present application (e.g., starting on page 12, line 18). As discussed with respect to Fig. 5, having the use or recent access registers or flags adjacent to memory cells allows efficient processing of a broadcast refresh in one implementation.

It is respectfully submitted that some of the independent claims now pending include recitations regarding use registers or recent-access flags being adjacent to memory cells or memory rows (see, e.g., claims 1, 11, 25, 32, 38, and 52). Accordingly, these independent claims should be patentable over Boyer. Additionally, claims 2-10, 12-18, 26, 28-31, 33-35, 29-40, and 53 which depend from the independent claims 1, 11, 25, 32, 38, and 52 should be patentable for at least similar reasons over Boyer, as well as additional recitations they contain.

Rejections Based on Ohsawa

Applicant would like to thank Examiner Verbrugge for clarifying the reasons for rejections over Ohsawa. It is, however, respectfully requested that the Examiner reconsider the rejections at least in light of the following remarks.

More particularly, Ohsawa's refresh flags are only provided by his "DRAM controller" (see, section 3.1, first sentence of the third paragraph). As a result, as discussed with reference to Boyer and Fig. 5 of the present application, Ohsawa can not benefit from the contemplated implementations associated with some of

the pending claims which stand rejected over Ohsawa (e.g., broadcast refresh). This is further illustrated by Ohsawa's use of the SRF (set refresh flag) in Fig. 5 and discussion in fourth paragraph of section 3.1. Also, referring to the third paragraph of section 3.1, Ohsawa states that the "refresh flag" (i.e., SRF of the fourth paragraph) is provided by the DRAM controller. Accordingly, Ohsawa teaches away from the claimed combination of features such as set forth in the claims that stand rejected over Ohsawa.

Additionally, the Examiner is kindly reminded of the previous Office Action which states that it "is not clear why Ohsawa mentions DRAM controller since he doesn't show it in the figures" or that a typical interpretation "doesn't seem to match Ohsawa's disclosure and figures." These discrepancies are clearly resolved by understanding that Ohsawa does not contemplate the use registers that are "adjacent" to memory cells. Moreover, it is respectfully submitted that Ohsawa intends Fig. 4 to be a mere illustration of high level "correspondence" between the refresh flag and each corresponding row, rather than a design criterion (where Ohsawa states in the second sentence of the third paragraph of section 3.1 that each "row is refreshed when the corresponding refresh flag is 1 (see Fig. 4)" [emphasis added]).

Furthermore, with respect to the last paragraph of page 11 of the outstanding Office Action which suggests that Fig. 2 of the present application is the same as Fig. 4 of Ohsawa, it is respectfully submitted that there are a lot more elements shown in Fig. 2 of the present application (e.g., memory controller,

refresh logic, etc.). As a result, it appears that Ohsawa's use of "memory unit" encompasses all elements of a memory system (e.g., a DRAM controller, cell array, etc.). However, Fig. 2 of the present application shows a memory device 16 which includes the use registers 24 and memory cells 22. This difference highlighted by the outstanding Office Action also shows that Ohsawa clearly didn't intend Fig. 4 to include a physical design criterion. Moreover, Fig. 2 is but one example of many implementations disclosed by the present application. For example, Fig. 4 shows a different implementation.

In addition, the outstanding rejections over Ohsawa only reject some of the independent claims (i.e., 1 and 11). Accordingly, it is respectfully submitted that the remaining independent claims are patentable over Ohsawa individually (i.e., 19, 25, 32, 38, and 52). Additionally, the remaining dependent claims 14-18, 26, 28, 29, and 31 that are rejected over Ohsawa should be allowable over Ohsawa individually for at least similar reasons as their respective independent claims.

Claims 19-24

Claim 19 as previously amended in part recites "use registers" and "refresh logic" on a memory device. As previously stated (e.g., in the last filed response), none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 19 (see also, e.g., the discussion above regarding Fig. 5 of the present application).

Claims 20-24 are dependent claims and should be allowable by virtue of their dependency on their respective base claim 19, as well as for the additional limitations they contain.

CONCLUSION

Applicant respectfully submits that claims 1-26, 28-35, 38-40, and 52-53 are in condition for allowance.

Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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